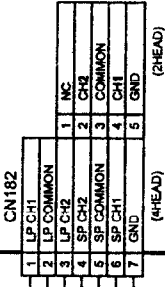
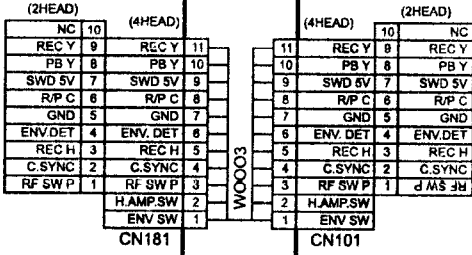
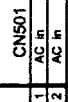
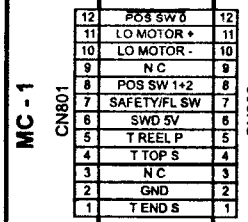
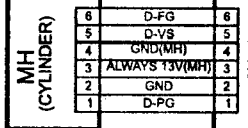
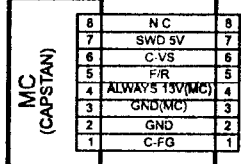
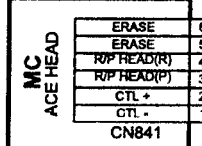
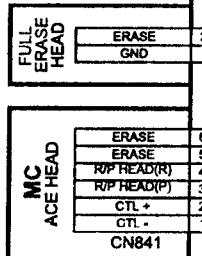
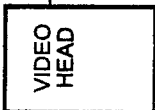


ПЛАТА VP - 1
(4HEAD/2HEAD PRE-AMP)

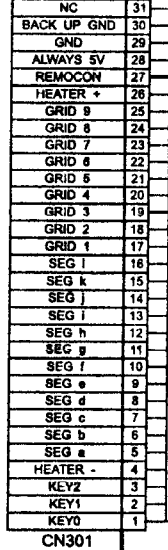


W0003

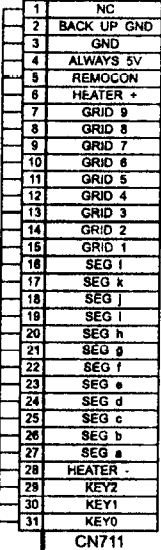


ОСНОВНАЯ ПЛАТА CP - 1

PW - A (POWER SUPPLY) TN - A (TUNER/MOD) SV - A (SERVO CIRCUIT) SY - A (SYSTEM CONTROL) AD - A (AUDIO) VD - A (VIDEO/OSD)



W0002

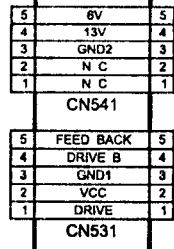


ПЛАТА TM - 1
DISPLAY (FLD) & SWITCH

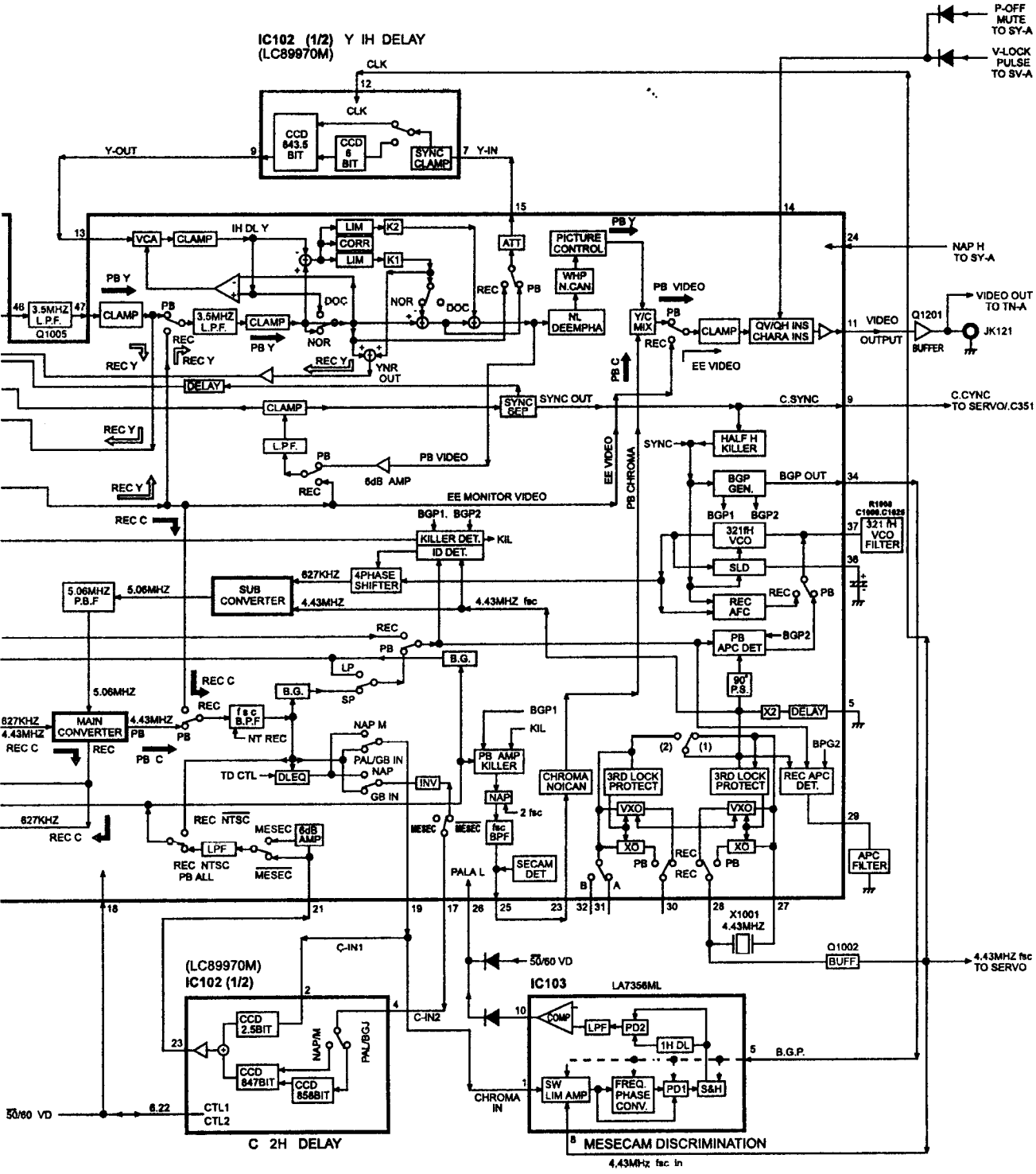
ОСНОВНЫЕ МЕХАНИЗМЫ
(MECHANISMS)

(MECHANISMS)

ПЛАТА PW - 1
(POWER CONTROL)



IC102 (1/2) Y IH DELAY
(LC89970M)



P-OFF MUTE TO SY-A
V-LOCK PULSE TO SY-A

NAP H TO SY-A

VIDEO OUT TO TN-A
JK121

C.SYNC TO SERVO/C351

R1008
C1008, C1020
321H VCO FILTER

X1001
4.43MHz

(LC89970M)
IC102 (1/2)

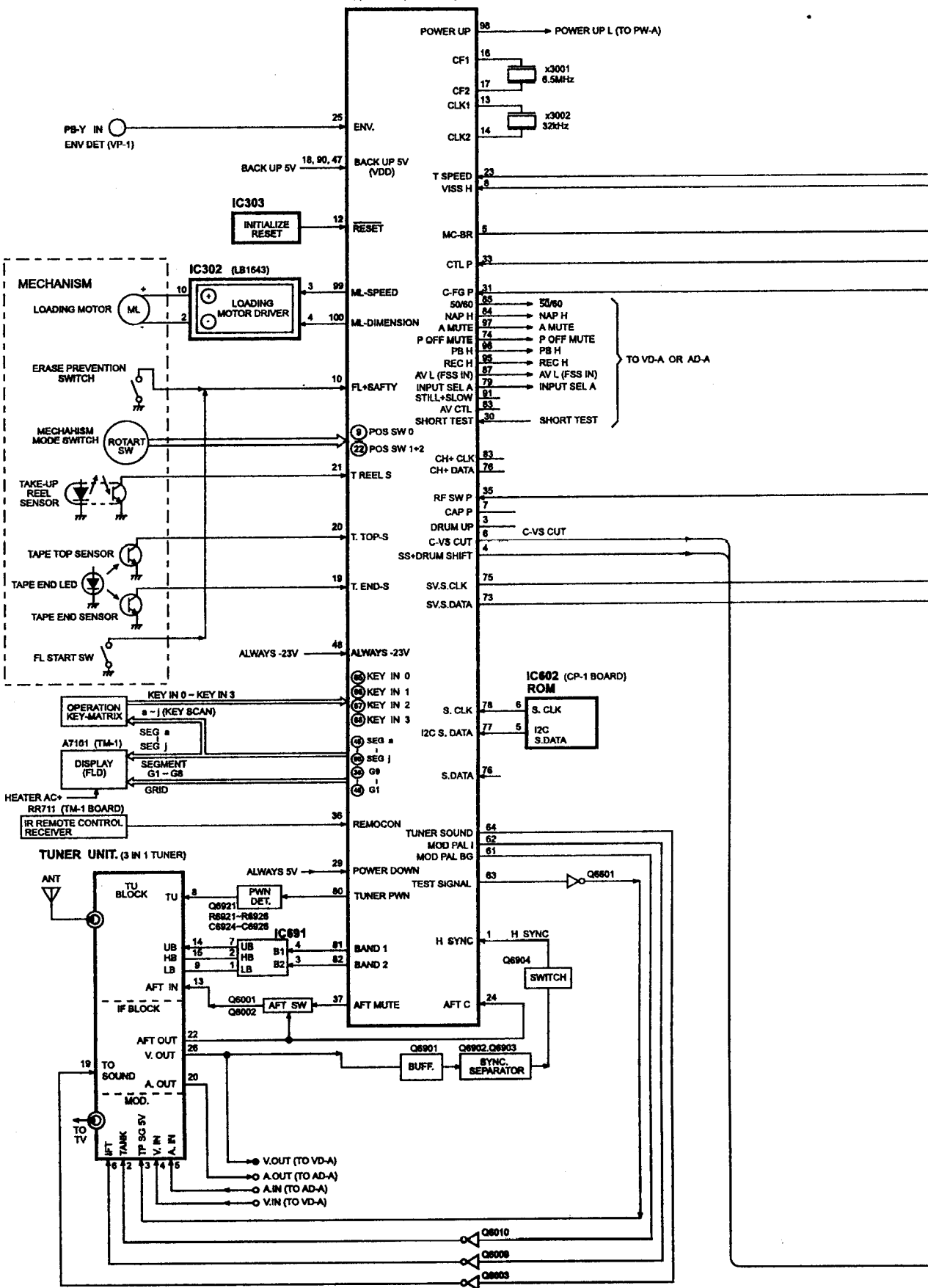
IC103
LA7356ML

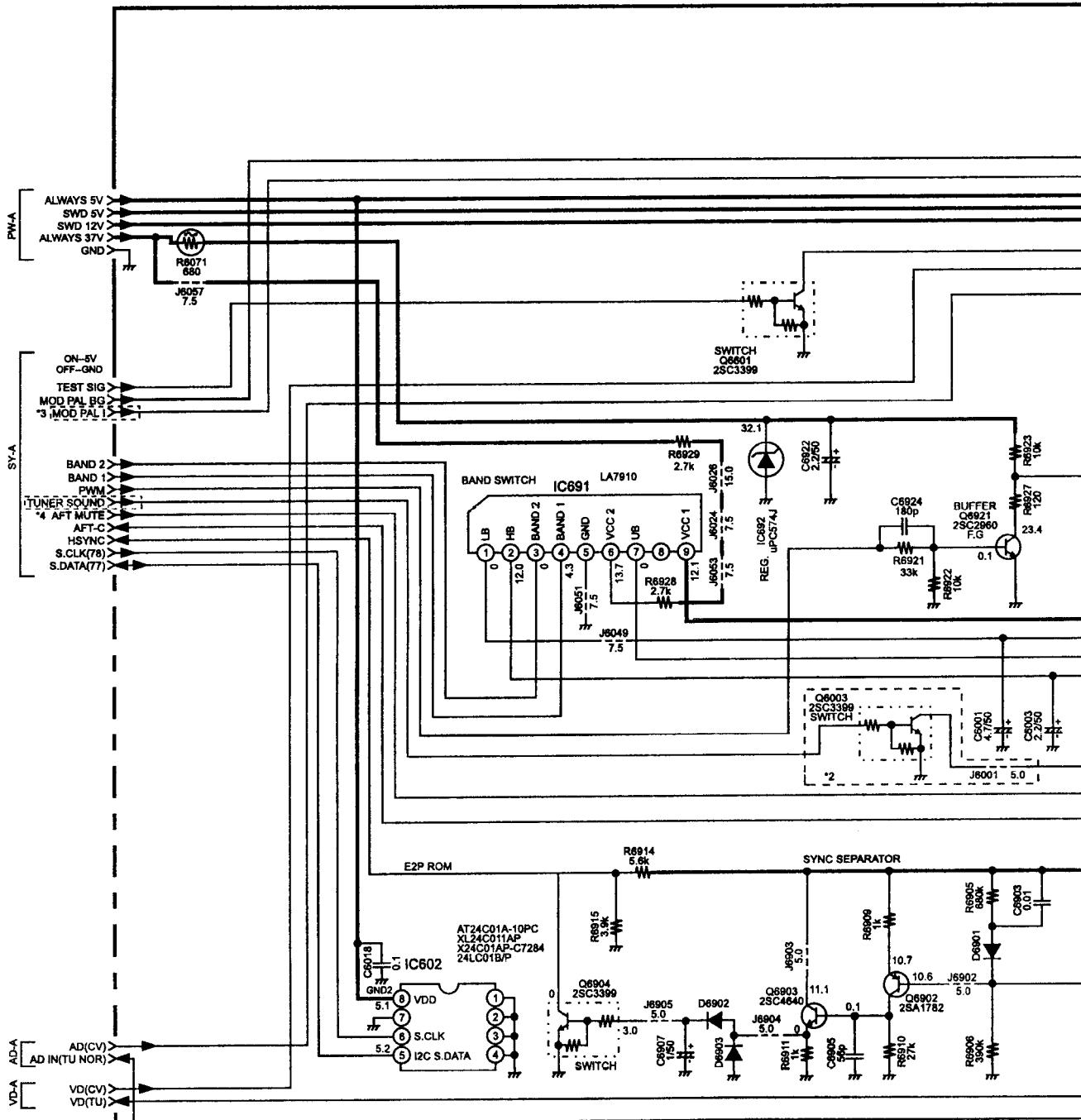
C 2H DELAY

MESECAM DISCRIMINATION

4.43MHz fsc in

IC301 MPU (CP-1 BOARD)
SYSTEM CONTROL, (LC866738) TIMER, TUNING CONTROL



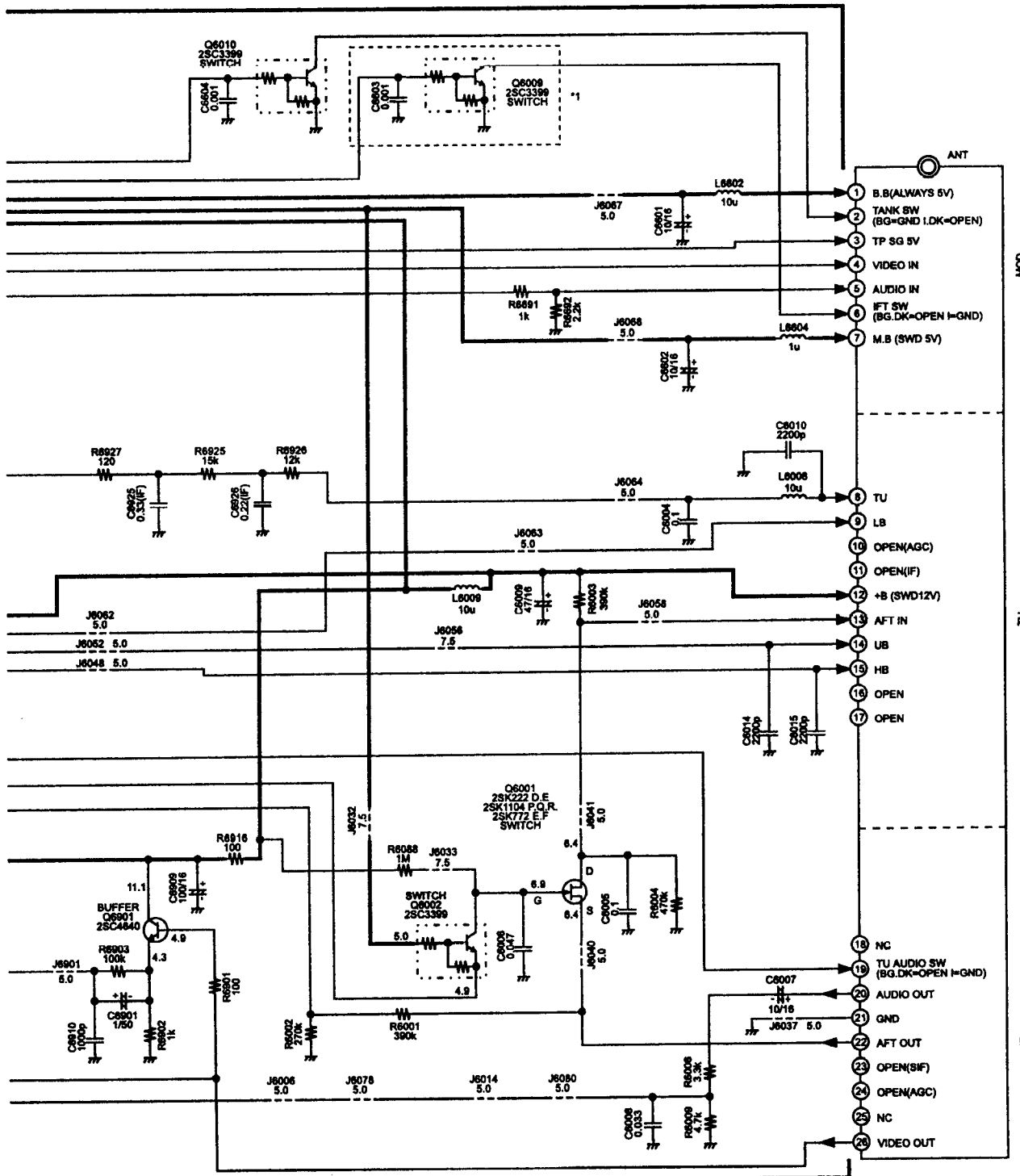


TN-A

NOTE

*1, *2, *3, *4 ... VHR-522 ONLY
 NOT SPECIFIED DIODES : 1SS133 or GMA01
 VOLTAGE : REC (PLAY) MODE

JP=6001-6099, 6601-6699, 6901-6999

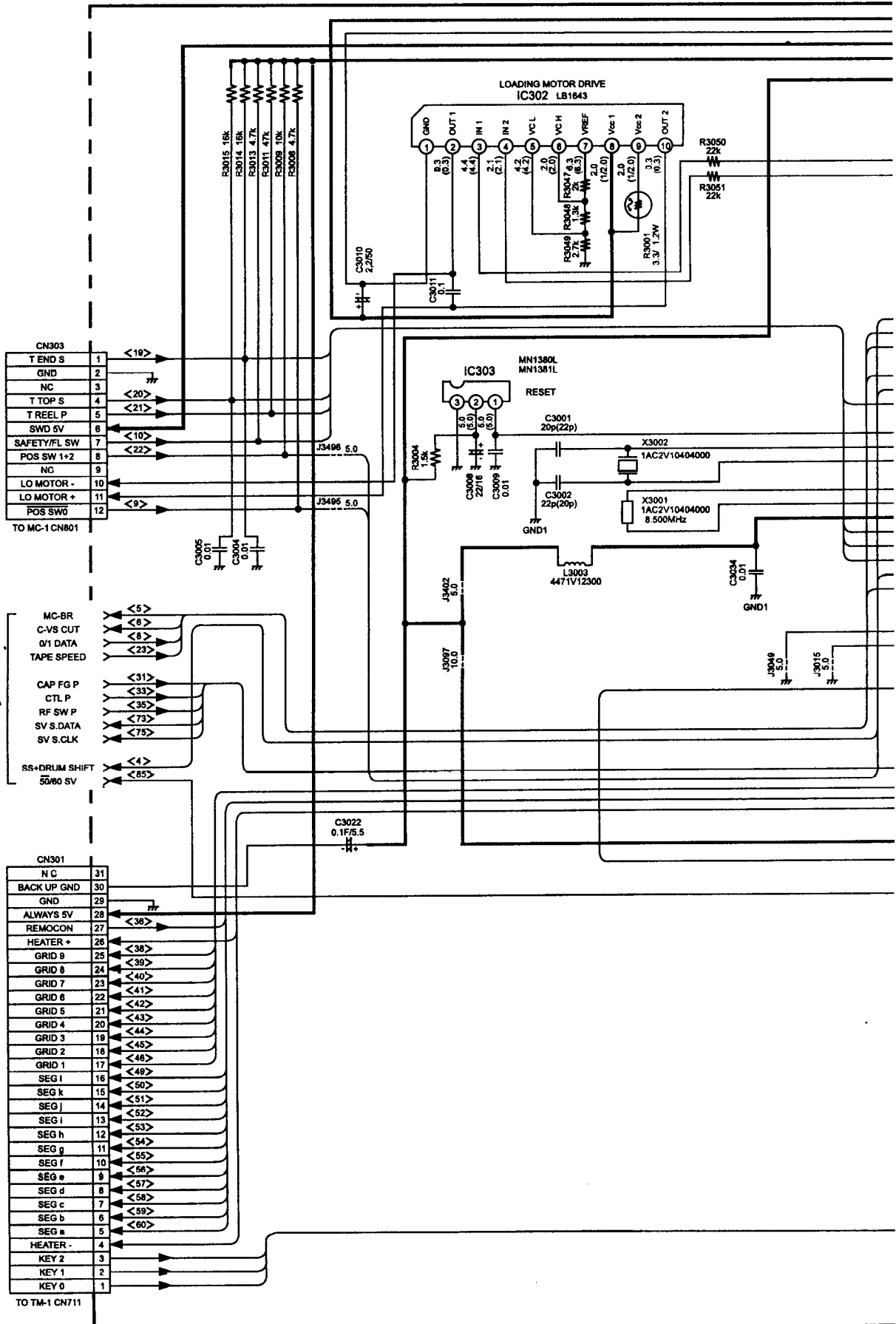


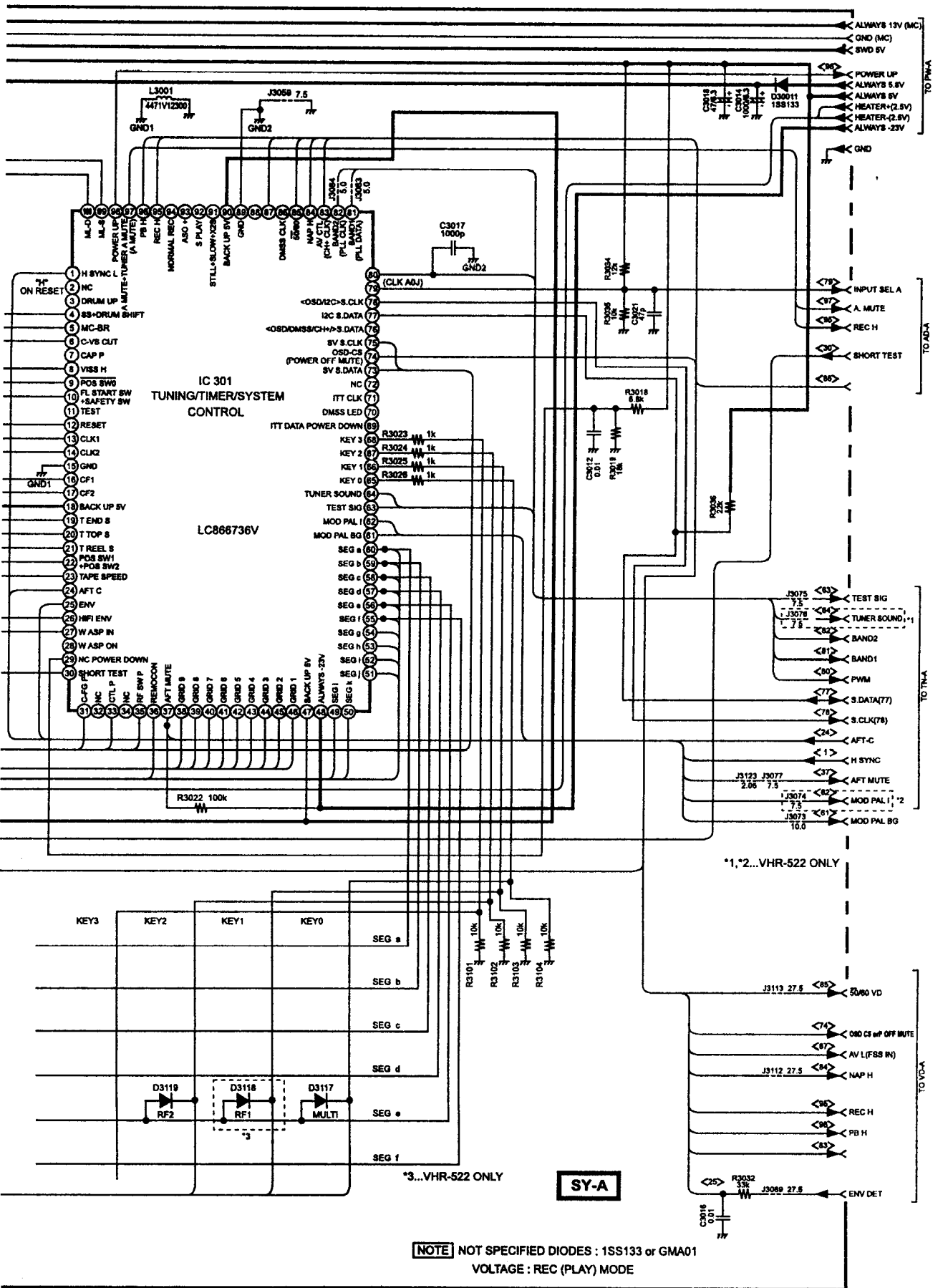
MOD.

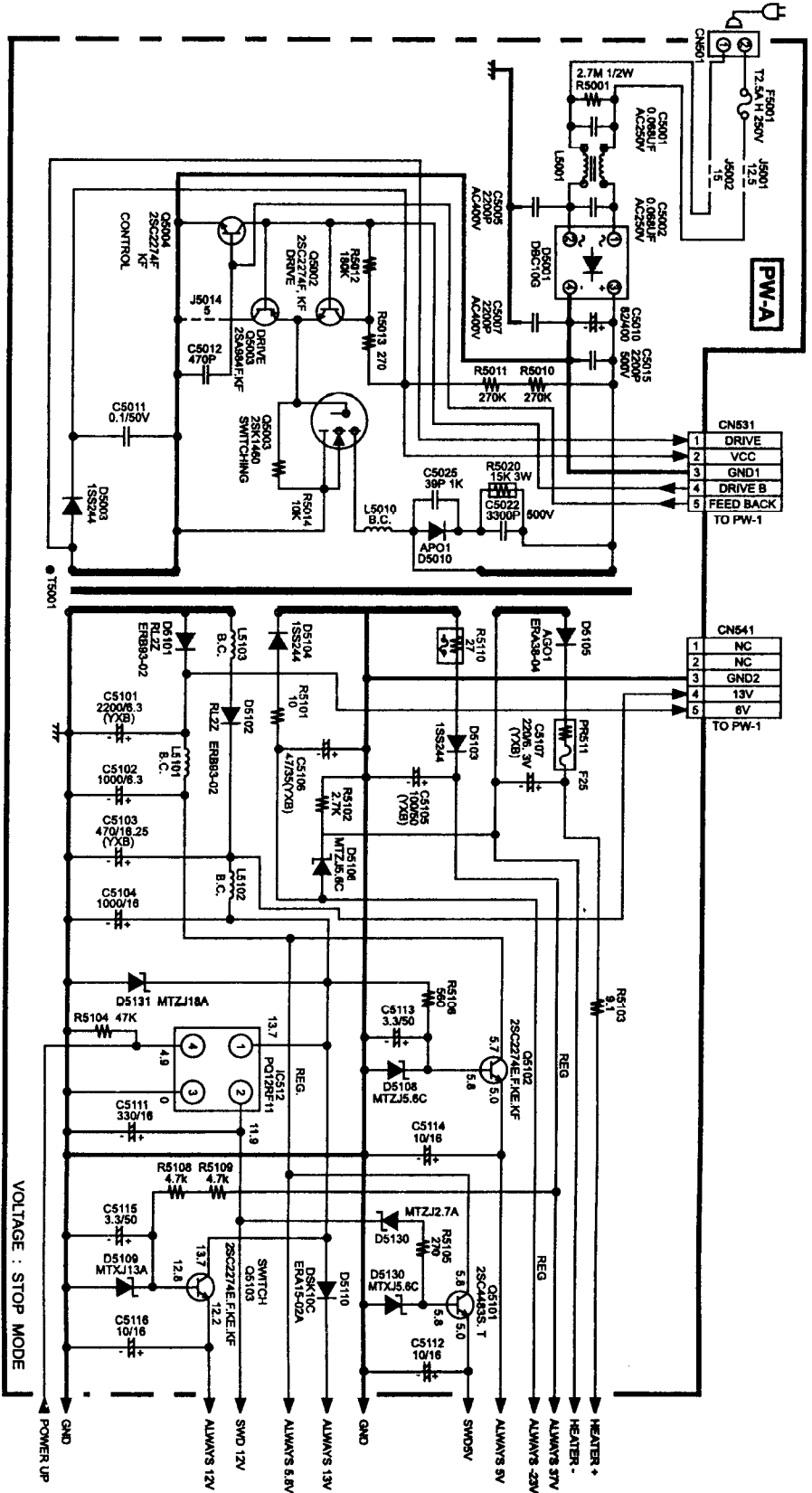
TU

F

- ANT
- 1 B.B.(ALWAYS 5V)
- 2 TANK SW (BG=GRND I.DK=OPEN)
- 3 TP SG 5V
- 4 VIDEO IN
- 5 AUDIO IN
- 6 IFT SW (BG.DK=OPEN I=GRND)
- 7 M.B (SWD 5V)
- 8 TU
- 9 LB
- 10 OPEN(AGC)
- 11 OPEN(IF)
- 12 +S (SWD12V)
- 13 AFT IN
- 14 UB
- 15 HB
- 16 OPEN
- 17 OPEN
- 18 NC
- 19 TU AUDIO SW (BG.DK=OPEN I=GRND)
- 20 AUDIO OUT
- 21 GND
- 22 AFT OUT
- 23 OPEN(SIF)
- 24 OPEN(AGC)
- 25 NC
- 26 VIDEO OUT







PWA

- CN531
- | | |
|---|-------------------|
| 1 | DRIVE |
| 2 | VCC |
| 3 | GND1 |
| 4 | DRIVE B |
| 5 | FEED BACK TO PW-1 |

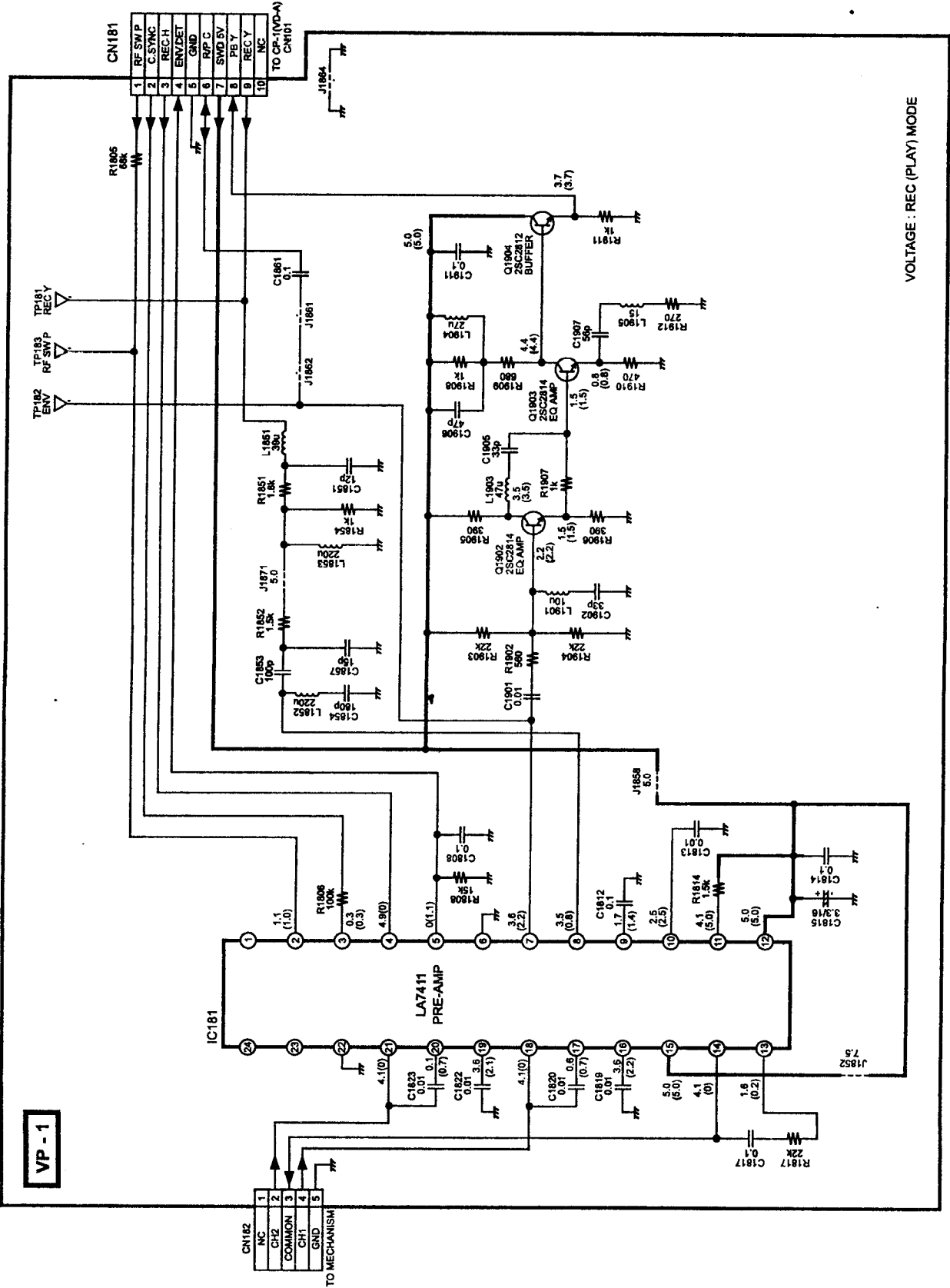
- CN541
- | | |
|---|------------|
| 1 | NC |
| 2 | NC |
| 3 | GND2 |
| 4 | 13V |
| 5 | 6V TO PW-1 |

VOLTAGE : STOP MODE

- POWER UP
- GND
- ALWAYS 12V
- ALWAYS 12V
- ALWAYS 5.8V
- ALWAYS 13V
- GND
- SWDSV
- ALWAYS 9V
- ALWAYS 3V
- HEATER -
- HEATER +
- ALWAYS 28V

TS901

VP - 1



VOLTAGE : REC (PLAY) MODE

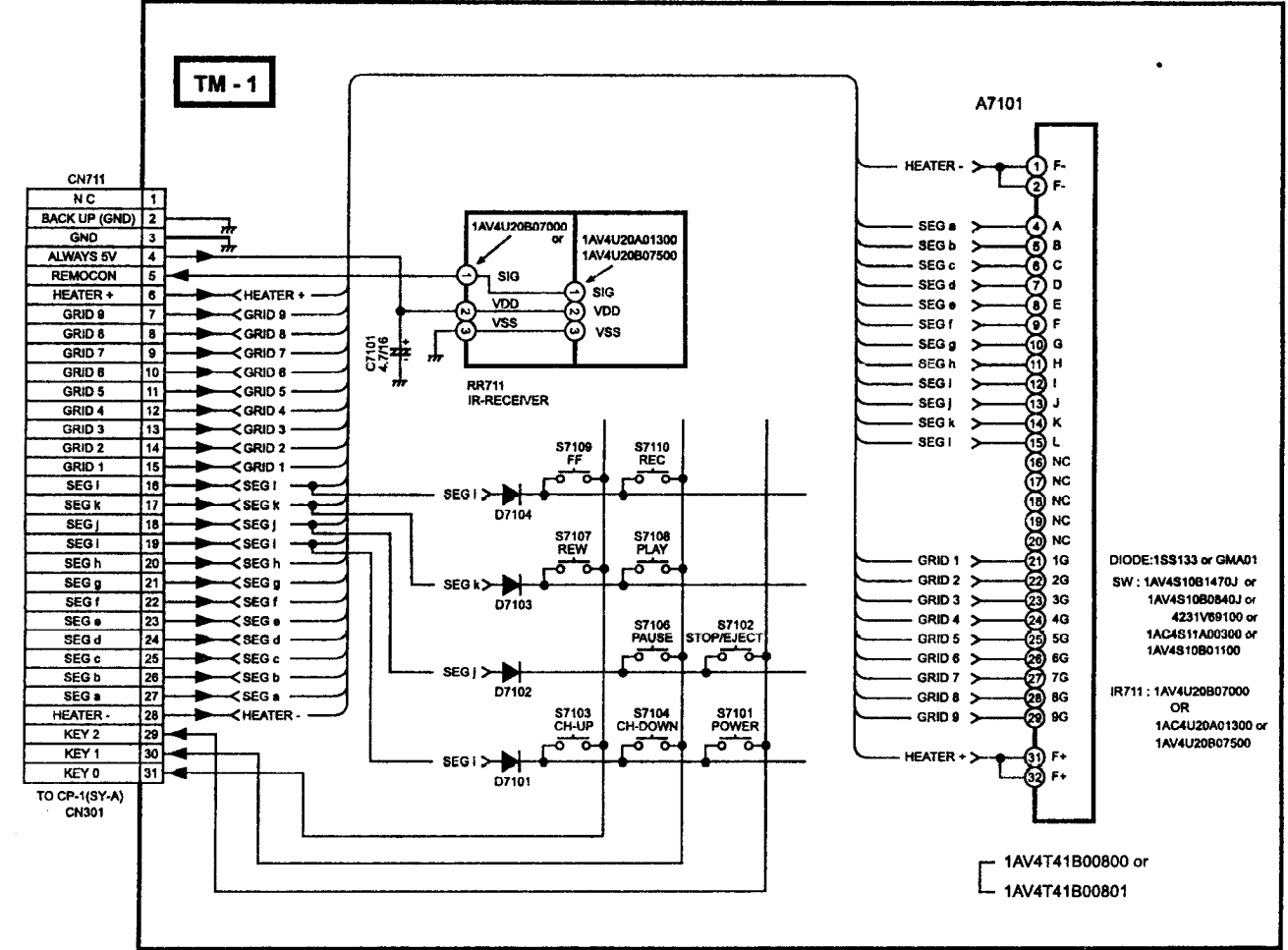
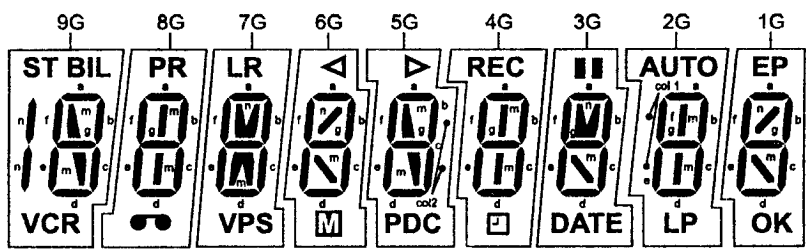


Рис. 4.15. Принципиальная схема платы оперативного управления и дисплея TM-1



a)

GRID \ SEGMENT	9G	8G	7G	6G	5G	4G	3G	2G	1G
a	ST	PR	L	◀	▶	REC	▬	AUTO	EP
b	n	—	n	n	—	—	n	—	n
c	a	a	a	a	a	a	a	a	a
d	b	b	b	b	b	b	b	b	b
e	c	c	c	c	c	c	c	c	c
f	d	d	d	d	d	d	d	d	d
g	e	e	e	e	e	e	e	e	e
h	f	f	f	f	f	f	f	f	f
i	g	g	g	g	g	g	g	g	g
j	m	m	m	m	m	m	m	m	m
k	BIL	—	VPS	—	col2	—	—	col1	—
l	VCR	☎	R	M	PDS	☐	DATE	LP	OK

б)